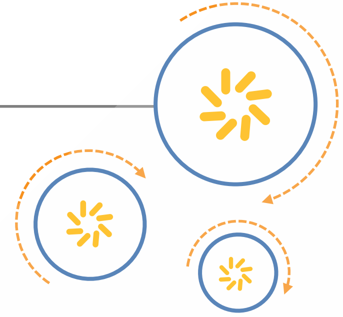

Qualcomm Atheros, Inc.

IPQ4018 Access Point SoC

Preliminary Device Specification

80-Y9347-18 Rev. C

August 19, 2015

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Revision history

Revision	Date	Description
A	May 2015	Initial release
B	July 2015	1. Section 3 “Electrical Specifications”: New. 2. Figure 4-3 and Table 4-2: Add Package B outline drawing. 3. Section 4.5 “Thermal Characteristics”: New
C	August 2015	1. Table 4-5 “Thermal Resistance”: Update θ_{JB} and θ_{JC}.

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1 Introduction

1.1 IPQ4018 general description

The IPQ4018 is a highly integrated system-on-chip (SoC) designed for high-performance, power-efficient, and cost-effective 2×2, 802.11ac, dual-band concurrent access-point applications. The SoC incorporates a quad-core ARM Cortex A7 processor, two dual-band, concurrent 802.11ac Wave-2 Wi-Fi subsystems, and a five-port Gigabit Ethernet Layer2/3/4 multilayer switch supporting line rate network address translation (NAT). It supports one USB3.0 and one USB2.0. It also supports miscellaneous interfaces such as I^{2}S, SPDIF, I^{2}C, SMI, UART, JTAG, etc., which can be configured as general purpose I/O pins. The block diagram in Figure 1-1 shows the major components of the SoC.

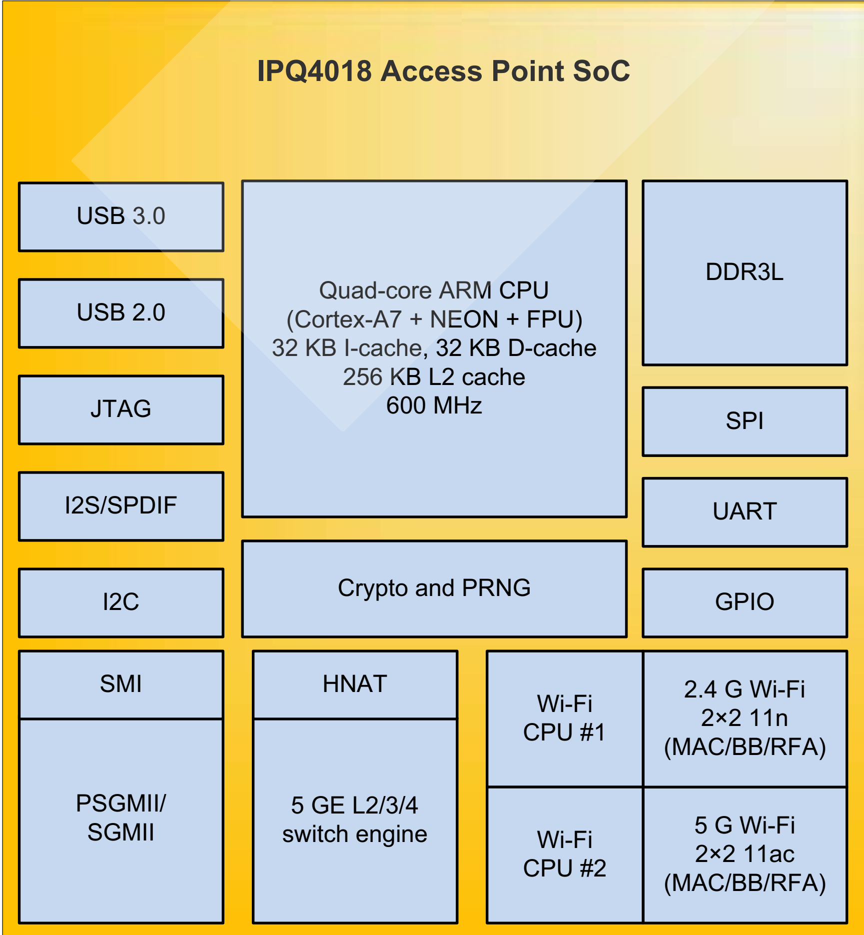

Figure 1-1 IPQ4018 functional block diagram

1.2 IPQ4018 features

- Quad-core ARM Cortex-A7 at 600 MHz
  - 32 KB instruction cache and 32 KB data cache per core
  - 256 KB L2 cache (shared)
  - Each core has NEON and FPU
  - Dynamic frequency scaling
  - Secure boot
- DRAM memory
  - JEDEC standard DDR3L SDRAM
  - Up to 256 MB
  - Supports 16-bit DDR interface
  - 533 MHz clock rate; 1066 MHz data rate
- Flash memory
  - SPI (x1b) flash
  - Supports NOR and/or NAND flash
  - Supports SPI mode 0, 1, 2, 3
  - Cache and non-cache mode read channel
- Dual Wi-Fi subsystem with Qualcomm® VIVE™ technology
  - On-chip dual-band concurrent (DBDC) 2×2 2G 802.11n (256QAM) and 2×2 5G 802.11ac Wi-Fi, supporting MU-MIMO beamforming techniques.
  - Feature compatible with QCA99xx Wi-Fi chips
  - Two dedicated CPUs for Wi-Fi offloading and feature growth
  - Cooperates with QFE19x2 front-end chips or 3rd-party front-end chipsets
  - Smart antenna diversity
- Network Subsystem
  - Integrated L2/3 multilayer switch/router
  - ACL (access control list) mask rules
  - Hardware network address translation (NAT) engine
  - Supports flow cookie
  - Traffic steering
  - Seamless integration with Linux network stack
  - Supports external gigabit Ethernet PHYs via PSGMII or SGMII
- Security
  - Crypto engine

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    - Encryption algorithms AES (128 and 256 bit key support) and DES/3DES
    - Authentication algorithms SHA1, SHA224 (the result of supporting SHA256), SHA256, and HMAC-SHA1 and HMAC-SHA2
    - XTS/CTR/CCM/CMAC mode for AES
    - CBC/ECB mode both for AES and DES/3DES.
  - Trust Zone
  - Pseudo-random number generator
- High-speed interfaces
  - 1× PSGMII/SGMII
  - 1 × USB3.0
  - 1 × USB2.0
- Miscellaneous
  - I²S, SPDIF, I²C, UART, SMI
  - JTAG
  - GPIO
- Package
  - 14 mm × 14 mm 180-pin Dual Row QFN package

1.3 Terms and abbreviations

Table 1-1 defines terms, abbreviations, and acronyms commonly used throughout this document.

Table 1-1 Terms and abbreviations

Term	Definition
ACL	Access control list
BB	Baseband
BLSP	BAM-enabled low-speed peripheral
DDR	Double data rate
GE	Gigabit Ethernet
GMII	Gigabit MII
LDO	Low drop-out (voltage regulator)
MII	Media-independent interface
NAT	Network address translation
PRNG	Pseudo-random number generator
PSGMII	Penta-SGMII
SGMII	Serial GMII

Table 1-1 Terms and abbreviations (cont.)

Term	Definition
SMI	Serial Management Interface
SoC	System on a chip
SPI	Serial peripheral interface
TDM	Time-division multiplexed (audio interface)

1.4 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

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2 Pin Definitions

2.1 IPQ4018 Pin map

Figure 2-1 shows a high-level view of the pin assignments.

The text within Figure 2-1 is difficult to read when viewing an 8½" by 11" hard copy. Other viewing options are available:

- Print that one page on an 11" by 17" sheet.
- View the graphic soft copy and zoom in.

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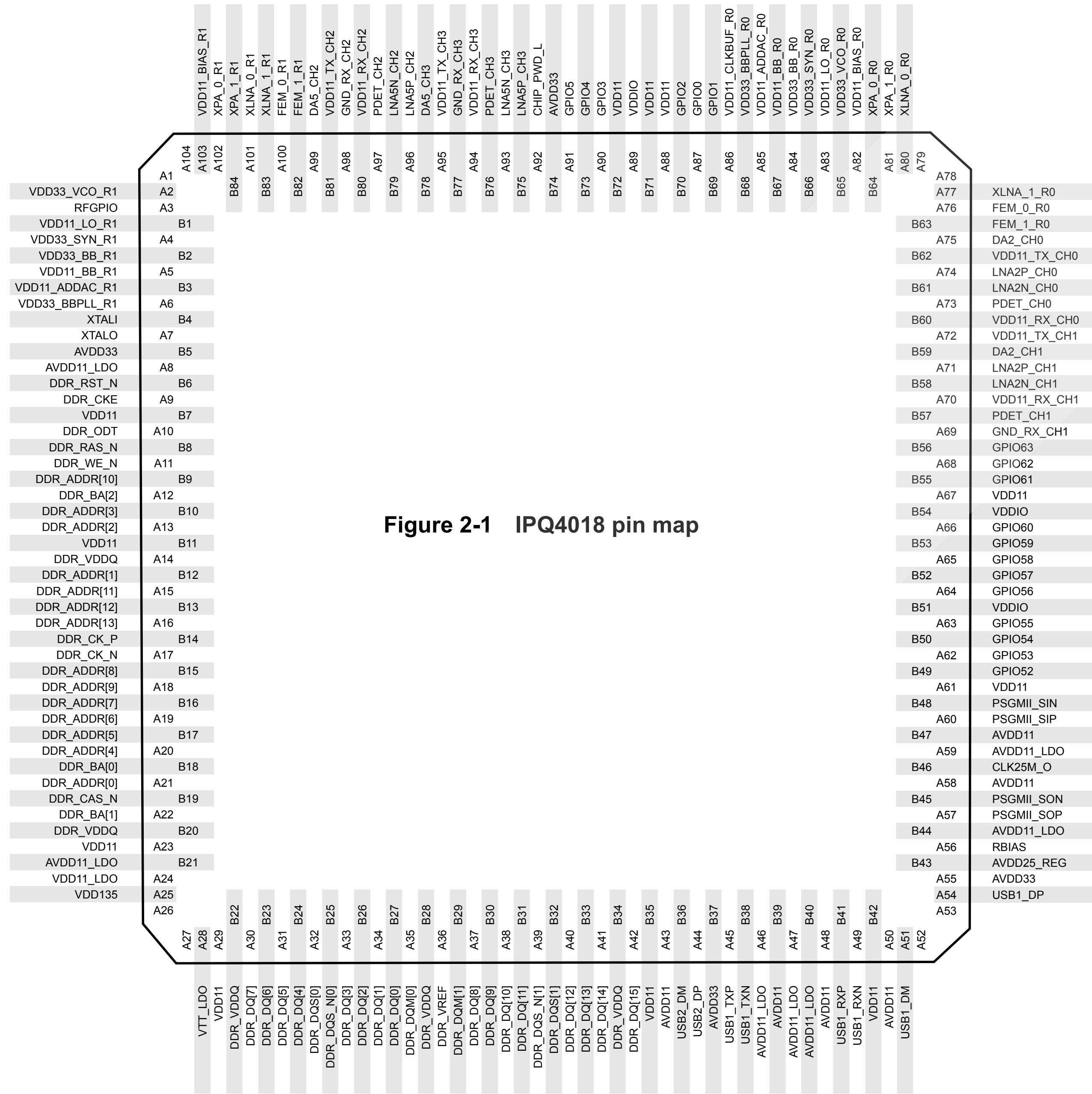

Figure 2-1 IPQ4018 pin map

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2.2 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
AI	Analog input
AO	Analog output
GND	Ground
NC	Not connected; leave disconnected
RF IN	RF input
RF Out	RF output
I	Digital input signal
O	Digital output signal
IO	Digital bidirectional signal

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2.3 Pin descriptions

Descriptions of pins are presented in the tables of this section. The pins are grouped by function.

2.3.1 Clock, power, and reset

Table 2-2 Clock, power, and reset

Pin ID	Pin Name	Voltage	Type	Functional Description
A43, A48, A50, A58, B39, B47	AVDD11	1.1	AI	1.1 V analog power
A8, A46, A47, A59, B21, B40, B44	AVDD11_LDO	1.1	AI	1.1 V analog power. Connect with pin A24 on board.
A55, B5, B37, B74	AVDD33	3.3	AI	3.3 V analog power
A23, A29, A61, A67, A88, B7, B11, B35, B42, B71, B72	VDD11	1.1	I	Digital power
A24	VDD11_LDO	1.1	O	1.1 V LDO output
A25	VDD135	1.35	I	Power input for VDD11_LDO and VTT_LDO. Route a dedicated wire from the 1.35 V switching regulator.
A89, B51, B54	VDDIO	3.3	I	Power for GPIO
A28	VTT_LDO	0.5 * VDD135	O	DDR termination voltage
B4	XTALI		I	Crystal oscillator input
A7	XTALO		O	Crystal oscillator output
A92	CHIP_PWD_L		I	Chip power-on reset.

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2.3.2 5G radio

In pin names and descriptions, "radio 1" or "R1" refers to the 5G radio. "Channel 2", "CH2", "Channel 3", and "CH3" are on the 5G radio.

Table 2-3 5G Radio Signals

Pin ID	Pin Name	Voltage	Type	Functional Description
B79 A96	LNA5N_CH2 LNA5P_CH2	1.1	IA	LNA differential input pair for chain 2
A93 B75	LNA5N_CH3 LNA5P_CH3	1.1	IA	LNA differential input pair for chain 3
A99	DA5_CH2	1.1	OA	DA single-ended output
B78	DA5_CH3			
A97	PDET_CH2	1.1	IA	PDET inputs
B76	PDET_CH3			
A102	XPA_0_R1		IO	External PA control
B84	XPA_1_R1			
A101	XLNA_0_R1		IO	External LNA control
B83	XLNA_1_R1			
A100	FEM_0_R1		IO	FEM control for CH0 of Radio 1
B82	FEM_1_R1			FEM control for CH1 of Radio 1

Table 2-4 5G Radio Power and Ground

Pin ID	Pin Name	Voltage	Type	Functional Description
A98	GND_RX_CH2		GND	
B77	GND_RX_CH3			
B3	VDD11_ADDAC_R1	1.1	I	1.1 V power supply for Radio 1
A5	VDD11_BB_R1			
A103	VDD11_BIAS_R1			
B1	VDD11_LO_R1			
B80	VDD11_RX_CH2			
A94	VDD11_RX_CH3			
B81	VDD11_TX_CH2			
A95	VDD11_TX_CH3			
A6	VDD33_BBPLL_R1	3.3	I	3.3 V power supply for Radio 1
B2	VDD33_BB_R1			
A4	VDD33_SYN_R1			
A2	VDD33_VCO_R1			

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2.3.3 2G radio

In pin names and descriptions, “radio 0” or “R0” refers to the 2G radio. “Channel 0”, “CH0”, “Channel 1”, and “CH1” are on the 2G radio.

Table 2-5 2G Radio Signals

Pin ID	Pin Name	Voltage	Type	Functional Description
A74	LNA2P_CH0		IA	LNA differential input pair for chain 0
B61	LNA2N_CH0			
A71	LNA2P_CH1		IA	LNA differential input pair for chain 1
B58	LNA2N_CH1			
A75	DA2_CH0		OA	DA single-ended output
B59	DA2_CH1			
A73	PDET_CH0		IA	PDET inputs
B57	PDET_CH1			
B64	XPA_0_R0		OA	External PA control
A81	XPA_1_R0			
A80	XLNA_0_R0		O	External LNA control
A77	XLNA_1_R0			
A76	FEM_0_R0			FEM control for CH0 of Radio 0
B63	FEM_1_R0			FEM control for CH1 of Radio 0

Table 2-6 2G Radio Power and Ground

Pin ID	Pin Name	Voltage	Type	Functional Description
A69	GND_RX_CH1		GND	
A85	VDD11_ADDAC_R0	1.1	I	1.1 V power supply for Radio 0
B67	VDD11_BB_R0			
A82	VDD11_BIAS_R0			
A86	VDD11_CLKBUF_R0			
A83	VDD11_LO_R0			
B60	VDD11_RX_CH0			
A70	VDD11_RX_CH1			
B62	VDD11_TX_CH0			
A72	VDD11_TX_CH1			
B68	VDD33_BBPLL_R0	3.3	I	3.3 V power supply for Radio 0
A84	VDD33_BB_R0			
B66	VDD33_SYN_R0			
B65	VDD33_VCO_R0			

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2.3.4 DDR3L

Table 2-7 16/8-bit DDR3L

Pin ID	Pin Name	Voltage	Type	Functional Description
A10	DDR_ODT			
B27	DDR_DQ[0]		I/O	DDR data[0:16]
A34	DDR_DQ[1]			
B26	DDR_DQ[2]			
A33	DDR_DQ[3]			
B24	DDR_DQ[4]			
A31	DDR_DQ[5]			
B23	DDR_DQ[6]			
A30	DDR_DQ[7]			
A37	DDR_DQ[8]			
B30	DDR_DQ[9]			
A38	DDR_DQ[10]			
B31	DDR_DQ[11]			
A40	DDR_DQ[12]			
B33	DDR_DQ[13]			
A41	DDR_DQ[14]			
A42	DDR_DQ[15]			
B14	DDR_CK_P		O	Differential clock (+)
A17	DDR_CK_N			Differential clock (-)
A9	DDR_CKE		O	Clock enable
B8	DDR_RAS_N			Chip select
B19	DDR_CAS_N			Chip select
A11	DDR_WE_N			Chip select
A35	DDR_DQM[0]			Data mask
B29	DDR_DQM[1]			
B18	DDR_BA[0]			Byte access[0:2]
A22	DDR_BA[1]			
A12	DDR_BA[2]			

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Table 2-7 16/8-bit DDR3L (cont.)

Pin ID	Pin Name	Voltage	Type	Functional Description
A21	DDR_ADDR[0]		O	DDR command/address[0:13]
B12	DDR_ADDR[1]			
A13	DDR_ADDR[2]			
B10	DDR_ADDR[3]			
A20	DDR_ADDR[4]			
B17	DDR_ADDR[5]			
A19	DDR_ADDR[6]			
B16	DDR_ADDR[7]			
B15	DDR_ADDR[8]			
A18	DDR_ADDR[9]			
B9	DDR_ADDR[10]			
A15	DDR_ADDR[11]			
B13	DDR_ADDR[12]			
A16	DDR_ADDR[13]			
A32	DDR_DQS[0]		I/O	Differential data strobe for byte 0 and 1 (+)
B32	DDR_DQS[1]			
B25	DDR_DQS_N[0]			Differential data strobe for byte 0 and 1 (-)
A39	DDR_DQS_N[1]			
B6	DDR_RST_N			Reset
A36	DDR_VREF	0.675	I	DDR RX reference voltage input
A14, B20, B22, B28, B34	DDR_VDDQ	1.35	I	DDR I/O power

2.3.5 USB 3.0 and 2.0

Table 2-8 USB 3.0 signals

Pin ID	Pin Name	Voltage	Type	Functional Description
A54	USB1_DP		AI, AO	USB HS data plus
A51	USB1_DM		AI, AO	USB HS data minus
B41	USB1_RXP		AI	USB SS receive data plus
A49	USB1_RXN		AI	USB SS receive data minus
B38	USB1_TXN		AO	USB SS transmit data minus
A45	USB1_TXP		AO	SS USB transmit data plus

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Table 2-9 USB 2.0 signals

Pin ID	Pin Name	Voltage	Type	Functional Description
A44	USB2_DP		AI, AO	USB HS data plus
B36	USB2_DM		AI, AO	USB HS data minus

2.3.6 Front-end

Table 2-10 Front-end

Pin ID	Pin Name	Voltage	Type	Functional Description
B43	AVDD25_REG	2.7	O	Power for pads and internal circuits.
A56	RBIAS	1.175	O	Connect to an off-chip 2.37 K resistor for IPP current generation.

2.3.7 PSGMII (Penta SGMII)/SGMII

Table 2-11 PSGMII

Pin ID	Pin Name	Voltage	Type	Functional Description
B46	CLK25M_O		O	Supply external PHY with 25 MHz clock
B45	PSGMII_SON	1.1	O	Differential negative output (6.25 GHz in PSGMII mode, 1.25 GHz in SGMII mode).
A57	PSGMII_SOP	1.1	O	Differential positive output (6.25 GHz in PSGMII mode, 1.25 GHz in SGMII mode).
B48	PSGMII_SIN	1.1	I	Differential negative input (6.25 GHz in PSGMII mode, 1.25 GHz in SGMII mode).
A60	PSGMII_SIP	1.1	I	Differential positive input (6.25 GHz in PSGMII mode, 1.25 GHz in SGMII mode).

2.3.8 GPIO Interface

Individual GPIOs are configured by software using GPIO_CFGn registers corresponding to the GPIO number.

Table 2-12 GPIO

Pin ID	Pin Name	GPIO_CFG. FUNC_SEL	Configurable Function	Voltage	Type	Functional Description
A87	GPIO0	0	GPIO	3.3		
		1	JTAG TDI[1]	3.3	I	JTAG test data in
		2	smart_ant0	3.3	IO	Smart antenna
B69	GPIO1	0	GPIO	3.3		
		1	JTAG TCK[1]	3.3	I	JTAG test clock
		2	smart_ant1	3.3	IO	Smart antenna

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Table 2-12 GPIO (cont.)

Pin ID	Pin Name	GPIO_CFG. FUNC_SEL	Configurable Function	Voltage	Type	Functional Description
B70	GPIO2	0	GPIO	3.3		
		1	JTAG TMS[1]	3.3	IO	JTAG test mode state
		2	smart_ant2	3.3	IO	Smart antenna
A90	GPIO3	0	GPIO	3.3		
		1	JTAG TDO[1]	3.3	Z	JTAG test data out
			boot_config(0)	3.3	I	
B73	GPIO4	0	GPIO	3.3		
		1	JTAG RST_N[1]	3.3	I	JTAG reset for debug
A91	GPIO5	0	GPIO	3.3		
		1	JTAG TRST_N[1]	3.3	I	JTAG test reset
		2	smart_ant3	3.3	IO	Smart antenna
B49	GPIO52	0	GPIO	3.3		
		2	MDC	3.3	I/O	Management Data Clock
			boot_config(13)			
A62	GPIO53	0	GPIO	3.3		
		2	MDIO	3.3	I/O	Management Data I/O
B50	GPIO54	0	GPIO	3.3		
		2	blsp_spi0_ss0_n(1)	3.3	O	SPI0 chipselect 0
A63	GPIO55	0	GPIO	3.3		
		2	blsp_spi0_mosi(1)	3.3	O	SPI0 Master-out Slave-in data
			boot_config(9)	3.3	I	
A64	GPIO56	0	GPIO	3.3		
		2	blsp_spi0_sck(1)		O	SPI0 serial clock
			boot_config(10)	3.3	I	
B52	GPIO57	0	GPIO	3.3		
		2	blsp_spi0_miso(1)		I	SPI0 Master-in Slave-out data
A65	GPIO58	0	GPIO	3.3		
		2	LED[2]	3.3	O	
		3	blsp_i2c0_sck(2)	3.3	IO	I^2C serial clock
		4	smart_ant0	3.3	IO	Smart antenna
		5	smart_ant6	3.3	IO	Smart antenna
B53	GPIO59	0	GPIO	3.3		
		2	blsp_i2c0_sda(2)	3.3	IO	I^2C serial data
		3	smart_ant1	3.3	IO	Smart antenna
		4	smart_ant7	3.3	IO	Smart antenna

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Table 2-12 GPIO (cont.)

Pin ID	Pin Name	GPIO_CFG. FUNC_SEL	Configurable Function	Voltage	Type	Functional Description
A66	GPIO60	0	GPIO	3.3		
		2	blsp_uart0_rxd(1)	3.3	I	UART receive data
		3	smart_ant2	3.3	IO	Smart antenna
		4	smart_ant4	3.3	IO	Smart antenna
		5	LED[0]	3.3	O	
		6	audio_txbclk	3.3	IO	Audio transmit bit clock
		7	audio_rxbclk	3.3	IO	Audio receive bit clock
B55	GPIO61	0	GPIO	3.3		
		2	blsp_uart0_txd	3.3	O	UART transmit data
		3	smart_ant3	3.3	IO	Smart antenna
		4	smart_ant5	3.3	IO	Smart antenna
		5	audio_txfsync	3.3	IO	Audio transmit frame sync
		6	audio_rxfsync	3.3	IO	Audio receiver frame sync
		7	LED[1]	3.3	O	
			boot_config(14)	3.3	I	
A68	GPIO62	0	GPIO	3.3		
		2	Chip_rst_out	3.3	O	Chip reset signal
		3	Wifi0_uart_txd	3.3	O	Wifi0 UART transmit data
		4	Wifi1_uart_txd	3.3	O	Wifi1 UART transmit data
			boot_config(11)	3.3	I	
B56	GPIO63	0	GPIO	3.3		
		2	Wifi0_uart_rxd	3.3	I	Wifi0 UART receive data
		3	Wifi1_uart_rxd	3.3	I	Wifi1 UART receive data
		4	Wifi1_uart_txd	3.3	I	Wifi1 UART transmit data
		5	Audio_txd[1]	3.3	O	Audio transmit data
		6	Audio_rxd	3.3	I	Audio receive data
		7	Audio_spdifout	3.3	O	Audio spdifout
		8	Audio_spdifin	3.3	I	Audio spdifin

1. Can also be activated by boot configuration.

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2.3.9 Boot configuration

Several GPIO signals can be used to configure the secure boot feature and boot device. They are sampled only during power-on reset. Table 2-13 shows the boot configuration signals.

Table 2-13 Boot configuration

Pin #	Pin name BOOT_CONFIG[n]	Alternate function	Type	Functional description
A64	10	GPIO56	I	Mode: 0 Native mode 1 Test mode
B49	13	GPIO52	I	Apps boot source. 0 Boot from SPI NOR 1 Boot from code RAM
A90	0	GPIO3	I	Apps authentication enable. Enables authentication for various AP code segments. Send to security control. 0 No authentication 1 Enable authentication
A63	9	GPIO55	I	Force USB boot. 0 Normal boot 1 Force boot ROM USB interface. Send to security control.
A68	11	GPIO62	I	JTAG boot enable. 0 GPIO0~GPIO5 are normal GPIOs; can be configured by the FUNC_SEL registers. 1 GPIO0~GPIO5 are occupied by JTAG interface; cannot be changed by the FUNC_SEL registers.
B55	14	GPIO61	I	Watchdog disable. Only valid in native mode. 0 Watchdog enabled 1 Watchdog disabled

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3 Electrical Specifications

More specifications will be added in future revisions of this document as the data become available.

3.1 Absolute maximum ratings

Operating the IPQ4018 under conditions beyond its absolute maximum ratings (listed in Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
	Junction temperature	–	125	°C
	Case temperature under bias	–	110	°C
	Storage temperature	-45	135	°C

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage, ambient temperature, and case temperature. The IPQ4018 meets all performance specifications when used within the recommended operating conditions (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating temperatures

Temperature	Description	Min	Typ	Max	Unit
Operating temperature (commercial)	Case temperature		–	110	°C

Table 3-3 Recommended operating voltages

NOTE The maximum and minimum data are preliminary and are subject to change based on characterization results. Typical voltages are voltages at the pins of the package.

Pin	Description	Min	Typ[1]	Max	Unit
General					
AVDD11		1.05	1.1	1.15	V
VDD11		1.05	1.1	1.15	V
AVDD11_LDO		1.08	1.1	1.12	V
VDD135		1.28	1.35	1.42	V
DDR_VDDQ		1.28	1.35	1.42	V
AVDD33		3.13	3.3	3.46	V
VDDIO		3.13	3.3	3.46	V
VTT_LDO		0.5 * VDD135 ± 40			mV
DDR_Vref		0.5 * VDD135 ± 20			mV
5G Radio					
VDD11_ADDAC_R1	1.1 V power supply for Radio 1	1.05	1.1	1.15	V
VDD11_BB_R1		1.05	1.1	1.15	V
VDD11_BIAS_R1		1.05	1.1	1.15	V
VDD11_LO_R1		1.05	1.1	1.15	V
VDD11_RX_CH2		1.05	1.1	1.15	V
VDD11_RX_CH3		1.05	1.1	1.15	V
VDD11_TX_CH2		1.05	1.1	1.15	V
VDD11_TX_CH3		1.05	1.1	1.15	V
VDD33_BBPLL_R1	3.3 V power supply for Radio 1	3.13	3.3	3.46	V
VDD33_BB_R1		3.13	3.3	3.46	V
VDD33_SYN_R1		3.13	3.3	3.46	V
VDD33_VCO_R1		3.13	3.3	3.46	V
2G Radio					
VDD11_ADDAC_R0	1.1 V power supply for Radio 0	1.05	1.1	1.15	V
VDD11_BB_R0		1.05	1.1	1.15	V
VDD11_BIAS_R0		1.05	1.1	1.15	V
VDD11_CLKBUF_R0		1.05	1.1	1.15	V
VDD11_LO_R0		1.05	1.1	1.15	V
VDD11_RX_CH0		1.05	1.1	1.15	V
VDD11_RX_CH1		1.05	1.1	1.15	V
VDD11_TX_CH0		1.05	1.1	1.15	V
VDD11_TX_CH1		1.05	1.1	1.15	V

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Table 3-3 Recommended operating voltages (cont.)

NOTE The maximum and minimum data are preliminary and are subject to change based on characterization results. Typical voltages are voltages at the pins of the package.

Pin	Description	Min	Typ[1]	Max	Unit
VDD33_BBPLL_R0	3.3 V power supply for Radio 0	3.13	3.3	3.46	V
VDD33_BB_R0		3.13	3.3	3.46	V
VDD33_SYN_R0		3.13	3.3	3.46	V
VDD33_VCO_R0		3.13	3.3	3.46	V

1. Typical voltages are voltages at the pins of the package.

3.3 48-MHz clock characteristics

A 48-MHz crystal with accuracy of +20 ppm may be used; for 5 MHz operation, +10 ppm is required.

Table 3-4 Reference requirements for 48 MHz crystal

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	—	—	48	—	MHz
Frequency trimming	—	-10	—	10	PPM
Duty cycle of output signal	—	48	—	52	%
Voltage swing	—	0.8	—	1.5	Vpp
Settling time	—	—	—	1	ms
Output phase noise (48 MHz)	f = 1 KHz	—	-123.5	-121.5	dBc/Hz
	f = 10 KHz	—	-145.5	-143.5	dBc/Hz
	f = 100 KHz	—	-156.5	-154.5	dBc/Hz
	f = 1000 KHz	—	-157.5	-155.5	dBc/Hz
Output harmonic spur	—	—	—	-40	dBc
Mode of vibration	—	Fundamental			

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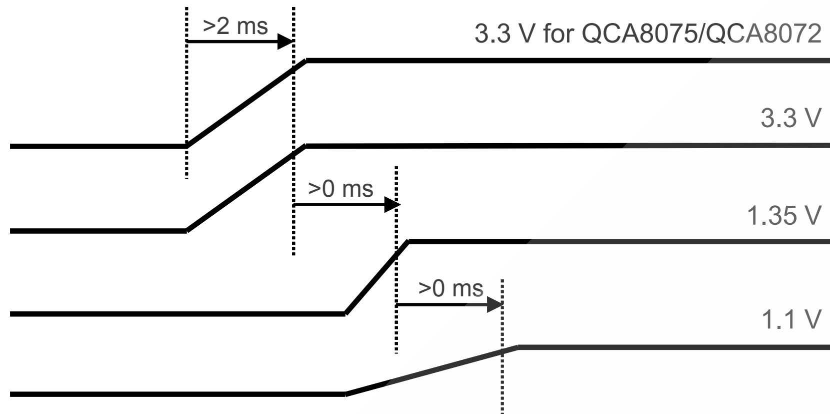
3.4 Power sequencing



4 Mechanical Information

The IPQ4018 uses 180-pin dual-row quad-flat no-leads (180DRQFN) package technology (see Figure 4-1).

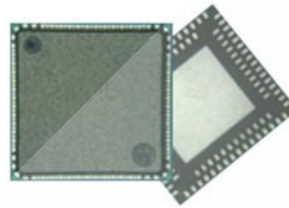


Figure 4-1 DRQFN package illustration

4.1 Device physical dimensions

Figure 4-2 shows the package drawing and Table 4-1 shows the dimensions for package A.
Figure 4-3 shows the package drawing and Table 4-2 shows the dimensions for package A.

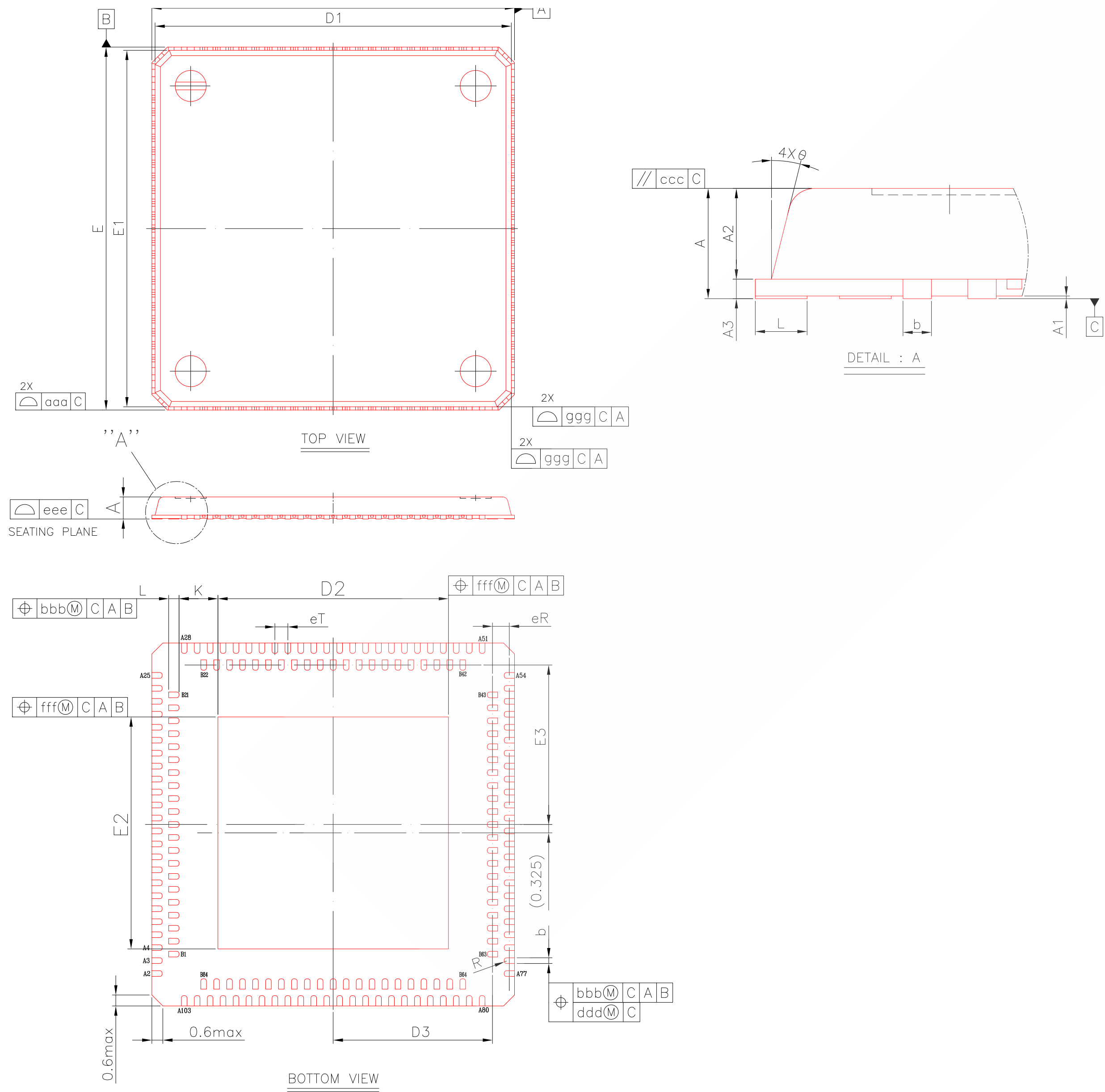


Figure 4-2 IPQ4018 180DRQFN package A details

Table 4-1 IPQ4018 180DRQFN package A dimensions

Dimension Label	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.65	0.70	0.75	mm
A3	0.15 REF			mm
b	0.18	0.22	0.30	mm
D/E	13.90	14.00	14.10	mm
D1/E1	13.75 BSC			mm
D2	8.80	8.90	9.00	mm
E2	8.85	8.95	9.05	mm
D3/E3	6.15 BSC			mm
eT	0.50 BSC			mm
eR	0.65 BSC			mm
L	0.30	0.40	0.50	mm
θ	5	---	15	°
K	0.20	---	---	mm
R	0.09	---		mm
aaa	0.10			mm
bbb	0.10			mm
ccc	0.10			mm
ddd	0.05			mm
eee	0.08			mm
fff	0.10			mm
ggg	0.20			mm

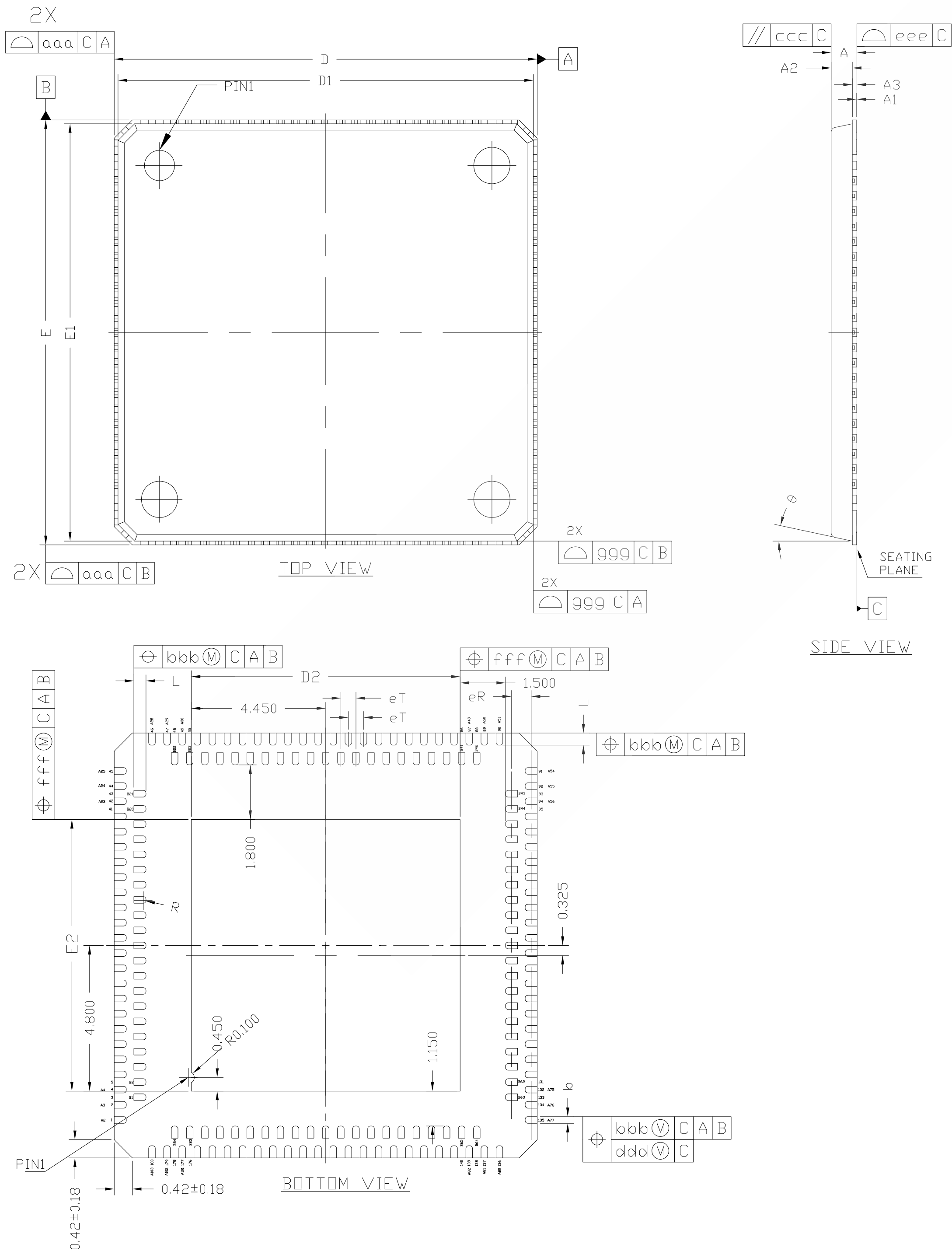


Figure 4-3 IPQ4018 180DRQFN package B details

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Table 4-2 IPQ4018 180DRQFN package B dimensions

Dimension Label	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.65	0.70	0.75	mm
A3	0.15 REF			mm
b	0.18	0.22	0.30	mm
D/E	13.90	14.00	14.10	mm
D1/E1	13.75 BSC			mm
D2	8.80	8.90	9.00	mm
E2	8.85	8.95	9.05	mm
eT	0.50 BSC			mm
eR	0.65 BSC			mm
L	0.30	0.40	0.50	mm
θ	5	---	15	°
R	0.09	---		mm
aaa	0.10			mm
bbb	0.10			mm
ccc	0.10			mm
ddd	0.05			mm
eee	0.08			mm
fff	0.10			mm
ggg	0.20			mm

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4.2 Part marking

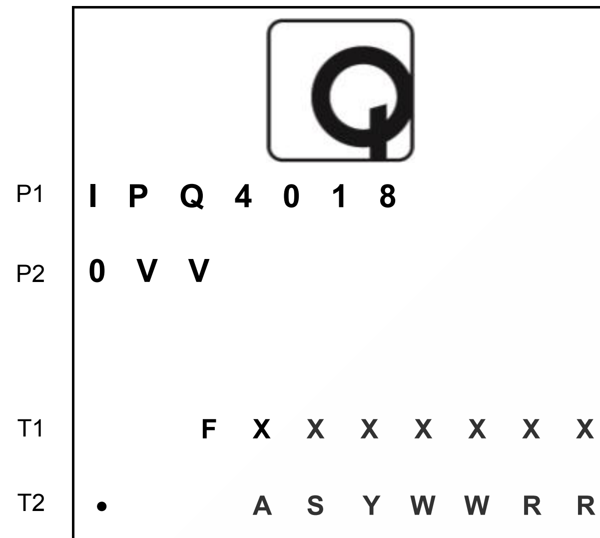

Figure 4-4 IPQ4018 marking (top view, not to scale)

Table 4-3 IPQ4018 marking line definitions

Line	Marking	Description
P1	IPQ4018	Product name
P2	*PBB*	P: configuration code = 0 BB: feature code = VV
T1	*FXXXXXXX*	F: fab code XXXXXXX = lot number
T2	*ASYWWRR*	A: assembly site code S: assembly sequence number Y: single, last digit of year WW: work week (based on calendar year) RR: revision code = 00

4.3 Device ordering information

Order numbers have the form shown in Figure 4-5.

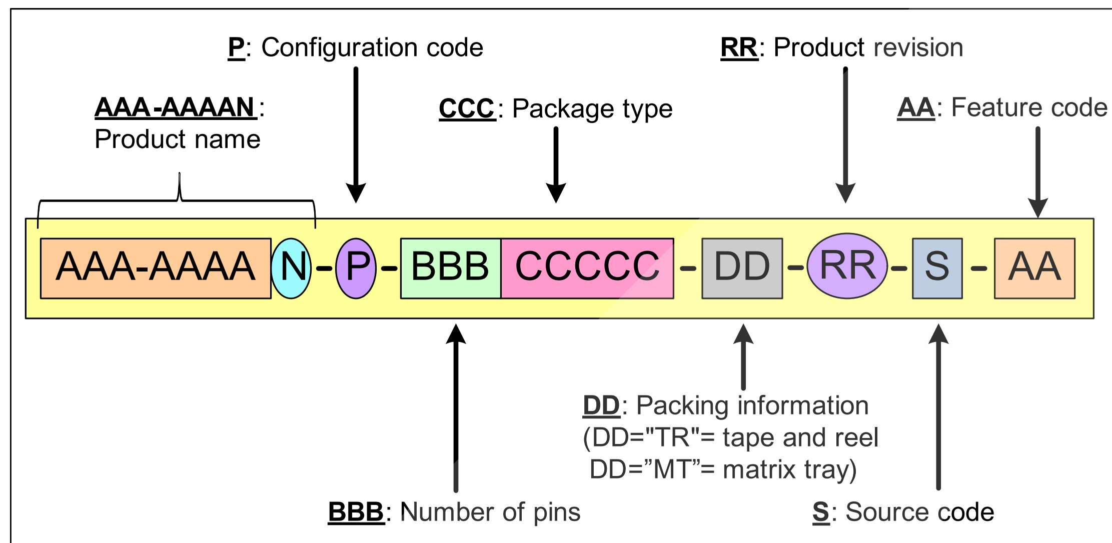

Figure 4-5 Device identification code

Table 4-4 shows the available order numbers.

Table 4-4 IPQ4018 order numbers

Order number	Description
IPQ-4018-0-180DRQFN-MT-00-0	RoHS & BrCl-free
IPQ-4018-0-180DRQFN-TR-00-0	RoHS & BrCl-free

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The IPQ4018 is classified as MSL3; the qualification temperature was 250ºC.

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4.5 Thermal characteristics

Table 4-5 Thermal Resistance

Parameter		Comment	Typical	Unit
θ_{JA}	Junction-to-Ambient	■ Jedec JESD51-2A ■ Jedec JESD51-7	19.3	°C/W
θ_{JB}	Junction-to-Board	■ Jedec JESD51-7 ■ Jedec JESD51-8 ■ Cold plate ring maintained at 25°C at top and bottom of PCB	13.3	°C/W
θ_{JC}	Junction-to-Case	■ No thermal vias ■ Jedec JESD51-7 ■ Jedec JESD51-8 ■ Cu block at top of package maintained at 25°C	4.5	°C/W
Ψ_{JT}	Junction-to-Top	■ Jedec JESD51-2A ■ Jedec JESD51-7	0.18	°C/W

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5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and reel information

The carrier tape system conforms to EIA-481 standards.

Simplified sketches of the IPQ4018 tape carrier are shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the IPQ4018 are as follows:

- Reel diameter: 330 mm
- Hub size: 178 mm
- Tape width: 24 mm
- Tape pocket pitch: 20 mm
- Feed: Single
- Units per reel: 2000

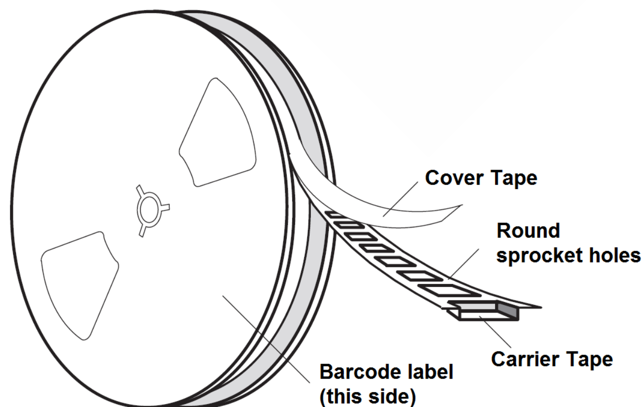

Figure 5-1 Tape orientation on reel

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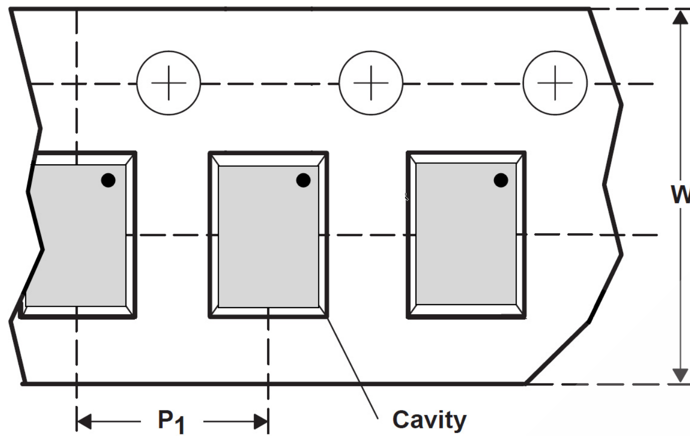
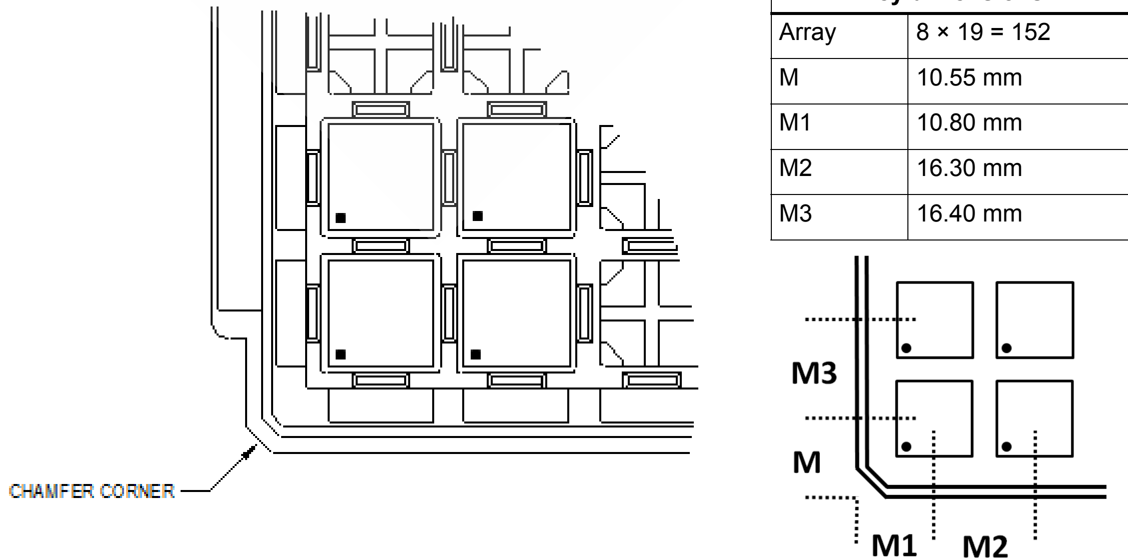


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

Matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of IPQ4018 contains up to 152 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	8 × 19 = 152
M	10.55 mm
M1	10.80 mm
M2	16.30 mm
M3	16.40 mm

Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

IPQ4018 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the IPQ4018 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the IPQ4018 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

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5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

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6 PCB Mounting Guidelines

Guidelines for mounting the IPQ4018 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The IPQ4018 device device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

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6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

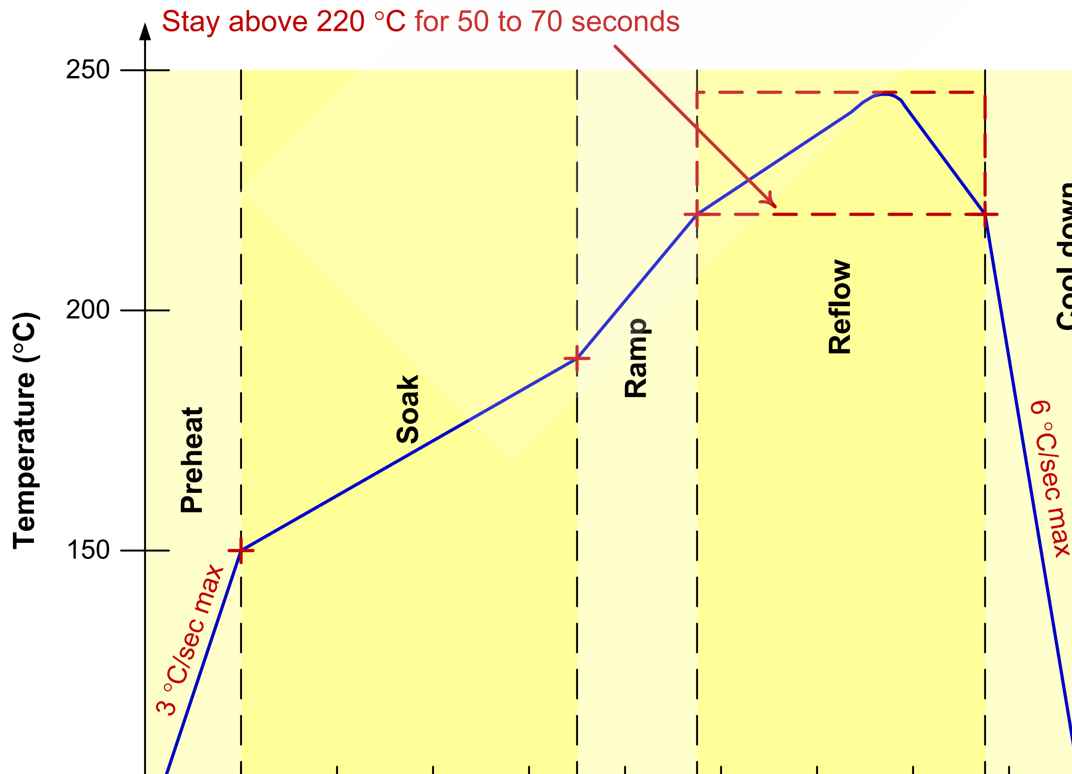

Figure 6-1 Typical SMT reflow profile

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6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

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